IT IS CLAIMED:

1. In a non-volatile memory device having a plurality of memory cells to be sensed in parallel, each memory cell having a source electrode, and the plurality of memory cells having their source electrodes tied together into a combined source line, a method of sensing comprising:

(a) providing a predetermined demarcation current value to discriminate between two memory states;

(b) sensing the plurality of memory cells in parallel;

(c) identifying those memory cells having conduction currents higher than said predetermined demarcation current value;

(d) inhibiting the conduction currents of those higher current memory cells after identifying all those higher current memory cells among said plurality of memory cells being sensed in parallel;

(e) repeating (b) to (d) for a predetermined number of times; and

(f) sensing the plurality of memory cells in parallel in a final pass.

2. The method of claim 1, wherein said predetermined number of times is zero.

3. The method of claim 1, wherein said predetermined number of times is one or greater.

4. The method of claim 1, wherein:

the conduction currents of said plurality of memory cells are sensed though a plurality of associated bit lines; and

said step of identifying those high current memory cells includes:

precharging said plurality of associated bit lines with a constant current source having a predetermined current limitation;

identifying those memory cells having conduction currents higher than said predetermined demarcation current value by their associated bit lines' precharging rates.

5. The method of claim 1, wherein:

said sensing is performed by an associated plurality of sense amplifier in parallel; and

said step of identifying those high current memory cells includes:

identifying those memory cells by using their associated sense amplifiers to compare their conduction currents relative to said predetermined demarcation current value.

6. The method of claim 1, wherein:

the conduction currents of said plurality of memory cells are sensed though a plurality of associated bit lines; and

said inhibiting the conduction currents includes pulling the associated bit lines of those memory cells to ground.

7. The method of claim 1, wherein:

said plurality of memory cells is non-volatile memory.

8. The method of claim 1, wherein:

said plurality of memory cells is flash EEPROM.

9. The method as in any one of claims 1-8, wherein:

each memory cell stores one bit of data.

10. The method as in any one of claims 1-8, wherein:

each memory cells stores more than one bit of data.

11. In a non-volatile memory device having a plurality of memory cells to be sensed in parallel, each memory cell having a source electrode, and the plurality of memory cells having their source electrodes tied together into a combined source line, a read system comprising:

a controller; and

a plurality of sensing circuits for sensing said plurality of memory cells in parallel, each sensing circuit further comprising:

a discriminator coupled to receive a conduction current of an associated memory cell, said discriminator discriminating whether the conduction current is higher or lower than a predetermined demarcation current value;

a latch being set to register the associated memory cell in response to said discriminator identifying a conduction current higher than said predetermined demarcation current value;

an inhibitor to turn off the conduction current of the associated memory cell;

an inhibitor enabler responsive to said plurality of sensing circuits having their discriminators completed their identifications and said latch being set; and wherein

said controller controls said plurality of sensing circuits to operate a predetermined number of times before reading out the determined memory state.

12. The read circuit as in claim 11, wherein said predetermined number of times is two.

13. The read circuit as in claim 11, wherein said predetermined number of times is greater than two.

14. The read circuit as in claim 11, further comprising:

a precharge circuit which is a constant current source having a predetermined current limitation; and wherein:

the conduction currents of said plurality of memory cells are sensed though a plurality of associated bit lines;

said precharge circuit precharging said plurality of associated bit lines; and

said plurality of sensing circuits identifying those memory cells having conduction currents higher than said predetermined demarcation current value by their associated bit lines' precharging rates.

15. The read circuit as in claim 11, wherein:

said plurality of sensing circuits identifying those memory cells having conduction currents by comparing their conduction currents relative to said predetermined demarcation current value.

16. The read circuit as in claim 11, wherein:

the conduction currents of said plurality of memory cells are sensed though a plurality of associated bit lines; and

said inhibitor turns off the conduction currents by pulling the associated bit lines of those memory cells to ground.

17. The read circuit as in claim 11, wherein:

said plurality of memory cells is non-volatile memory.

18. The read circuit as in claim 11, wherein:

said plurality of memory cells is flash EEPROM.

19. The read circuit as in any one of claims 11-18, wherein:

each memory cell stores one bit of data.

20. The read circuit as in any one of claims 11-18, wherein:

each memory cell stores more than one bit of data.

21. In a non-volatile memory device having a plurality of memory cells to be sensed in parallel, each memory cell having a source electrode, and the plurality of memory cells having their source electrodes tied together into a combined source line, a read system comprising:

a controlling means; and

a plurality of sensing circuits for sensing conduction currents of said plurality of memory cells in parallel, each sensing circuit further comprising:

means for discriminating whether the conduction current is higher or lower than a predetermined demarcation current value;

means for registering the associated memory cell in response whenever its conduction current is identified to be higher than said predetermined demarcation current value;

inhibitor means for inhibiting the conduction current of the associated memory cell;

means for enabling said inhibitor means responsive to said plurality of sensing circuits having their discriminators completed their identifications and said latch being set; and wherein

and

means for inhibiting the associated memory cell with said higher conduction current; and wherein

said controlling means operating said plurality of sensing circuits a predetermined number of times before reading out the sensed memory state in a final pass.

22. The read circuit as in claim 21, wherein said predetermined number of times is two.

23. The read circuit as in claim 21, wherein said predetermined number of times is greater than two.

24. The read circuit as in claim 21, further comprising:

a precharge circuit which is a constant current source having a predetermined current limitation; and wherein:

the conduction currents of said plurality of memory cells are sensed though a plurality of associated bit lines;

said precharge circuit precharging said plurality of associated bit lines; and

said plurality of sensing circuits identifying those memory cells having conduction currents higher than said predetermined demarcation current value by their associated bit lines' precharging rates.

25. The read circuit as in claim 21, wherein:

said plurality of sensing circuits identifying those memory cells having conduction currents by comparing their conduction currents relative to said predetermined demarcation current value.

26. The read circuit as in claim 21, wherein:

the conduction currents of said plurality of memory cells are sensed though a plurality of associated bit lines; and

said inhibitor means turns off the conduction currents by pulling the associated bit lines of those memory cells to ground.

27. The read circuit as in claim 21, wherein:

said plurality of memory cells is non-volatile memory.

28. The read circuit as in claim 21, wherein:

said plurality of memory cells is flash EEPROM.

29. The read circuit as in any one of claims 21-28, wherein:

each memory cell stores one bit of data.

30. The read circuit as in any one of claims 21-28, wherein:

each memory cell stores more than one bit of data.

31. A non-volatile memory, comprising:

an array of memory storage units;

a plurality of sense amplifiers for sensing a group of memory storage units in parallel;

each of said plurality of sense amplifiers having predetermined properties dependent on a set common parameters and a set of control signals; and

a reference circuit sharing a common environment with said plurality of sense amplifier, said reference circuit for calibrating said set of common parameters with respect to the common environment and generating said set of control signals accordingly so that said plurality of sense amplifiers are controlled to have its predetermined properties enforced.